Application Note:

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Thermal Considerations of QFN and Other Exposed-Paddle Packages

Note: This application note is a summary and compilation of information based on the references mentioned at the end of this document. This information is neither tested nor guaranteed by Maxim Integrated Products. Individuals should examine the published references for details about the source and test procedures used to obtain this information.

MAXIM High-Frequency/Fiber Communications Group

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1 Overview/Introduction

As we move forward in the high-tech world, one of the most visible changes we notice is the miniaturization of electronic devices. From laptops to PDAs, electronic devices are shrinking. With high frequency devices, small size is not only convenient but it is also a necessity of the design. The size of fiber optic receivers, transmitters, transceivers, and transponders continue to shrink. The small area and close proximity of ICs in these modules demands small packages with excellent thermal properties. The introduction of the exposed paddle has helped to reduce package size and improve the thermal characteristics of the device.

Many of Maxim Fiber Optic and High Frequency products incorporate exposed paddles in their packages (Figure 1). The exposed-paddle packages effectively decrease the thermal resistance, which in turn provides excellent heat dissipation from the die. Package sizes can be decreased and power dissipation increased with the exposed paddle which in turn leads to substantial system level improvements.

In most cases the exposed paddle also acts as electrical ground. This provides improved electrical performance by minimizing package ground lead inductance. The decreased ground inductance improves edge speeds and output waveforms.

Better thermal characteristics, smaller package sizes and improved electrical performance make exposed-paddle packages ideal for high-speed data applications.

Improper connection of the exposed paddle can lead to increased junction temperature, increased power consumption and decreased electrical performance. Long-term reliability issues, increased failure rate, or total IC failure can also occur.

This application note will give a brief introduction to thermal theory and general layout considerations that can be applied in order to obtain the benefits of the exposed-paddle package. A worst-case example of performance degradation due to improper use of the exposed paddle will also be provided.

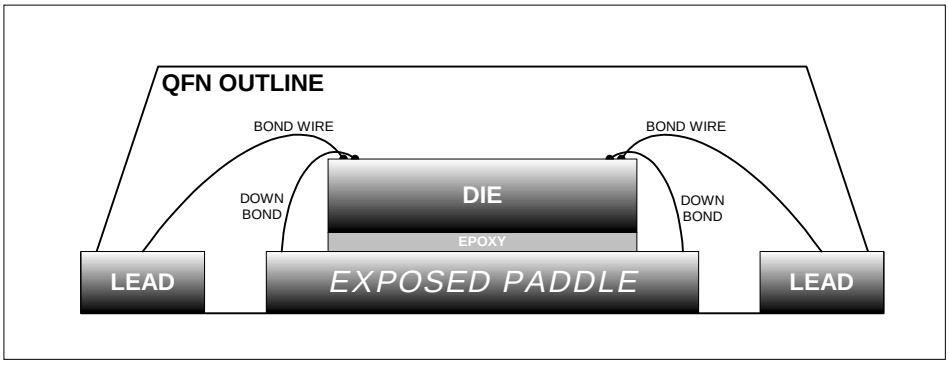

Figure 1. Internal Connection to the Exposed Paddle

2 General Thermal Theory

Thermal properties of a device can often be expressed as components in an electrical circuit (Figure 2). Power dissipation is modeled as a current source, thermal resistance is modeled as electrical resistance and temperature is modeled as a voltage. The models are not perfect, but they do provide easy steady-state evaluation of thermal problems using familiar circuit analysis techniques. The model shown does not apply to transient thermal resistance. For more information on transient thermal resistance see the application note, "Transient Thermal Resistance – General Data and Its Use" (Reference 9).

2.1 General Definitions:

- **θ_{JA}** – Thermal resistance between junction and ambience given in °C/W (Figure 2). The θ_{JA} specifies the increase in junction temperature (T_J) above ambient temperature (T_A) for every watt of power. Mathematically θ_{JA} is given as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} = \frac{T_J - T_A}{P_D} \text{ °C/W}$$

- **θ_{JC}** – Thermal resistance between junction temperature (T_J) and case temperature (T_C) (Figure 2).

- **θ_{CA}** – Thermal resistance between case temperature (T_C) and ambient temperature (T_A) (Figure 2).

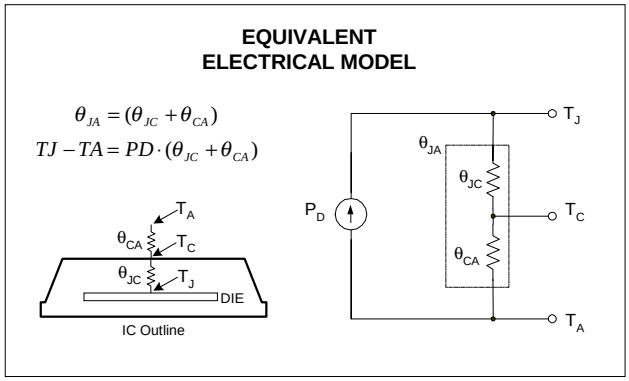

Figure 2: Equivalent Electrical Model

- **Maximum Continuous Power Dissipation** – Maximum continuous power that can be dissipated at the junction of the IC by the package (Figure 3). This value is indicated in the IC's data sheet in the *Absolute Maximum Ratings* section. The value is specified at a given temperature (usually maximum ambient operating temperature) with a particular derating factor ($1/\theta_{JA}$) calculated from specific test conditions. (See the following section, 2.3 JEDEC Standard Boards.) This value is indicative of the package and not the die. It simply states how much power can be dissipated by the package, and is not representative of the power of the die. If operation is performed above the specified temperature (T_{Amax}), the package is unable to dissipate the maximum continuous power rating and must be derated (Figure 3).

- **Maximum Junction Temperature** – Highest temperature of the junction before damage or increased failure rate occurs (Figure 3).

- **Derating Factor** – Factor that limits the power dissipation for temperatures above the specified maximum operating temperature (Figure 3). The derating factor is equivalent to $1/\theta_{JA}$ mW/°C. Maximum continuous power is derated to zero at maximum junction temperature.

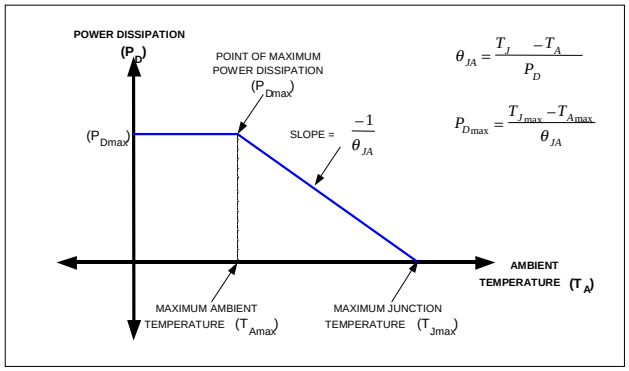

Figure 3: Power Dissipation vs. Ambient Temperature

- **Conduction** – Heat transfer through direct contact (For Example: IC package to a heat sink).

- **Convection** – Heat transfer by air movement across the device or PCB (laminar or turbulent).

- **Radiation** – Heat transfer to ambient by IR radiation (no airflow).

2.2 Thermal Resistance

The thermal resistance of an IC is affected by many parameters, some of which can be changed by a system designer to obtain improved heat transfer characteristics. Other parameters have a direct relation to the IC package.

θ_{JC} is derived from specific characteristics of the IC package such as die size, lead frame material/design and package body material. These values are specific to the IC and can not be improved with system changes by the end user.

θ_{CA} is directly related to system level variables. Forced-air cooling, package mounting, trace width, external heat sinks and many other variables all affect the total thermal resistance of an IC.

The combined thermal resistance of θ_{JC} and θ_{CA} is known as θ_{JA} (thermal resistance from junction to ambiance). This helps in understanding the scope of the θ_{JA} value when evaluating IC packages. As mentioned above, θ_{JA} is dependent upon many external system level variables. The θ_{JA} value given in data sheets is relevant only for specific, standardized conditions and may not reflect actual results in a final product. For this reason, θ_{JA} should be used as a relative number when evaluating the thermal dissipation performance of an IC package.

2.3 JEDEC Standard Boards

In general, the IC industry measures θ_{JA} using tightly constrained system characteristics from the JEDEC standard (References 12-22). The JEDEC standard uses two test boards to measure thermal resistance. There is a high K (four layer board, two power planes) and a low K (two layer board, no internal power planes). The most important features of the two boards are shown in Table 1 (References 15, 19). Experiments have shown a 30% to 45% decrease in the thermal resistance when using a high K board (Reference 11).

Table 1: JEDEC General Specs of High/Low K boards (References 15, 19)

Test Board	Low K board (inch)	High K board (inch)
Trace Thickness	0.0028 (2 oz.)	0.0028 (2 oz.)
Trace Length	0.98	0.98
PCB Thickness	0.063	0.063
PCB Width	3	3
PCB Length	4.5	4.5
Power/Ground Plane Thickness	No Internal Copper Plane	0.0014 (2 planes, 1 oz.)

If the designed PCB has the exact same properties of the JEDEC test board and your test environment is the same, you can expect the same thermal resistance as that given in the data sheet. In practice, only a relative determination of the packages thermal characteristics can be concluded from the θ_{JA} value.

2.4 Heat Transfer

Most of the heat generated by an IC is conducted to the PCB and then radiates from the PCB to the ambient (Figure 4). It is a characteristic of surface-mount packages tested in standard environment that upwards of 70% of the generated heat flows to the air through the board. The presence of metal planes in the test PCB can increase the value to over 90% (Reference 2). Heat is transferred to the PCB from the leads and package. An exposed-paddle package improves the heat transfer efficiency by creating a low thermal resistive path to the PCB.

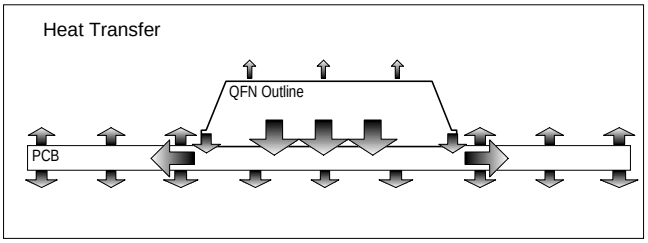

Figure 4: Heat Transfer

3 PCB Layout Considerations

General guidelines will be given, which will aid in designing a PCB that uses exposed-paddle packages. The suggestions should be evaluated and optimized for each individual process and design. Many factors affect the overall thermal characteristics of a design and can be calculated using thermal analysis software.

3.1 System Level

The amount of heat dissipation needed for a design depends on:

1. Power of the IC.

2. Ambient temperature

3. PCB material properties and PCB geometry

4. Amount of airflow or forced air

5. PCB IC densities

Not all ICs that have exposed paddles are high power devices. The exposed paddle has many attractive features other than thermal transfer and does not directly indicate a high power device. The exposed-paddle package does indicate the ability to dissipate more heat than a standard package. It is important to examine the typical and maximum power of a device, as well as the power that can be dissipated by the package.

When heat transfer is an issue, multi-layer boards with dedicated power planes are recommended. The multi-layer boards typically have a larger thermally conductive area for heat removal due to the internal copper planes (Reference 7).

Heat concentration due to multiple devices and the general environment in which the part operates should also be considered at the system level.

There is no quick and easy way of estimating the board size and properties needed for proper thermal dissipation, but the following suggestions will aid in the PCB design of a system that uses exposed-paddle packages.

3.2 Heat Transfer from the Exposed Paddle.

The exposed paddle provides a low thermal resistance path for heat transfer to the PCB. This low thermally resistive path carries the majority of the heat away from the IC. The PCB is effectively the heat sink for the IC.

The exposed paddle should be attached to the ground plane for proper thermal and electrical performance. (Refer to the IC specific data sheet for more information.) To create an efficient path the exposed paddle is soldered to a thermal landing, which is connected to the ground plane by thermal vias (Figure 5).

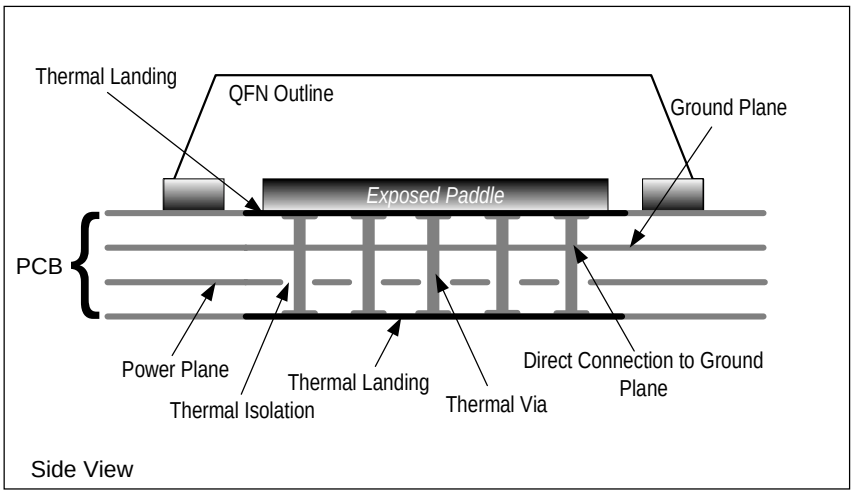

Figure 5: Side view of PCB, Exposed Paddle, Thermal Vias and Thermal Landing

3.2.1 Thermal Landing

The thermal landing is a copper layer on the component side of the PCB (Figure 5). Also, it is recommended to place a thermal landing on the opposite side of the PCB. This will improve the thermal transfer to ambient and increase the thermally conductive area.

The thermal landing should be at least as large as the exposed paddle and can be made larger depending on the amount of free space from the exposed paddle to other pin landings (Reference 5).

3.2.2 Thermal Vias

The thermal landing is connected to the ground plane with thermal vias (Figure 6). The thermal vias direct heat from the thermal landing to the ground plane as well as to ambient through the bottom of the PCB. Multiple vias improve the heat transfer away from the IC and also improve the electrical connection to ground (when applicable). A 1.0 to 1.2mm pitch is the recommended spacing for the vias in most applications (Reference 5).

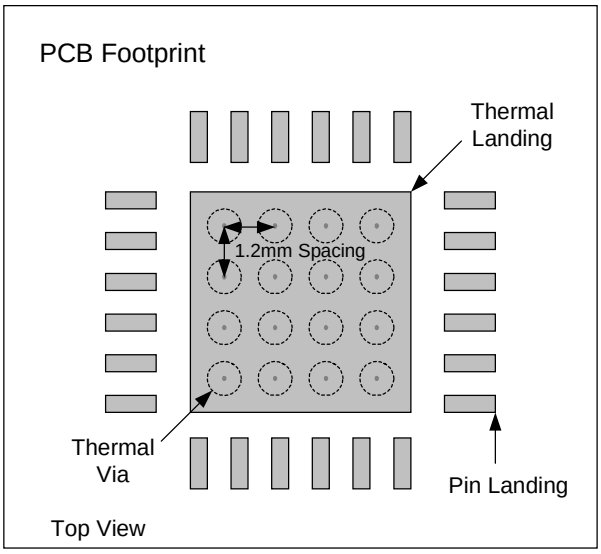

Figure 6: PCB Footprint and Thermal Landing

The thermal vias should be plated (1oz Copper) and have a small barrel diameter (.30 to .33mm) (Reference 5) so that the hole is substantially closed during the plating process (Figure 7). If the diameter of the vias after plating is too large, solder will be pulled away from the exposed paddle (solder wicking) during the reflow process.

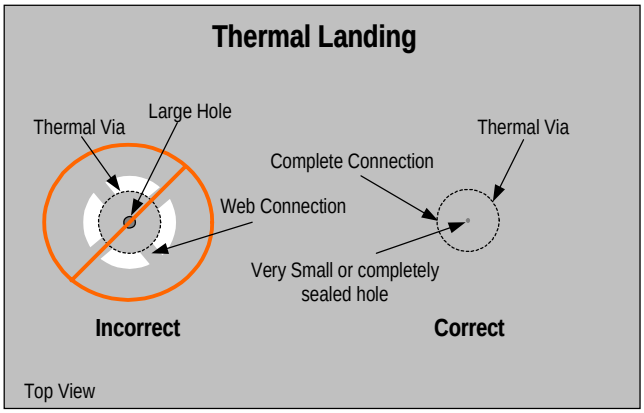

Figure 7: Thermal Landing and Thermal Via

Large amounts of solder wicking due to large hole diameters in the thermal vias will decrease the solder joint between the exposed paddle and the thermal landing (In typical applications, the exposed paddle should have a solder joint area of 90%) (References 6, 7).

Note: The term "thermal via" is also commonly given to a "web-constructed via," a via with web construction to the surrounding plane. These are often used in through-hole applications to facilitate the soldering of a pin to a large plane. The web-constructed via has a larger thermal resistance to the plane. For this reason, do not use web connection from the via to the thermal landing or the ground plane (Figure 7). Web construction decreases the thermal transfer properties of the vias from the thermal landing to the ground plane.

3.2.3 Ground Plane

The ground plane and surrounding material direct heat away from the IC (Figure 4). A ground plane of 1oz copper is recommended (Reference 7). As mentioned earlier, the size of this plane is dependent upon many different system variables. The size of the ground plane and other thermal considerations should be considered early in the development phase of a project.

4 Board Mounting

The procedure for mounting an exposed-paddle package is similar to standard mounting procedures. The process is shown in Figure 8 (Reference 5).

For more information regarding assembly and rework see reference 5, pages 5-7 and reference 6, pages 11-14.

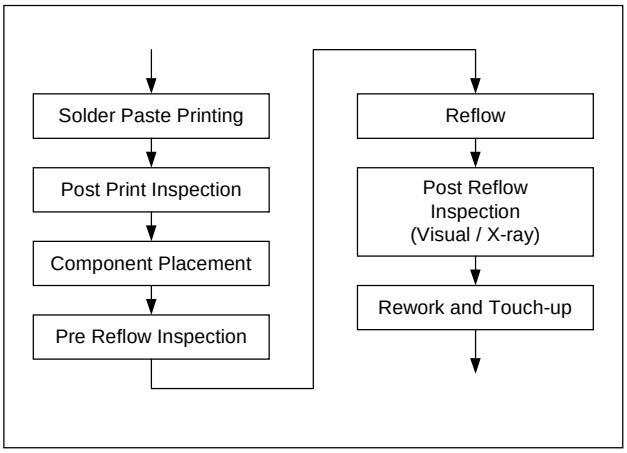

Figure 8: Board Mounting Process Flow (Reference 5)

5 Thermal Example

The following experiments were performed to illustrate the thermal effects of the exposed paddle. Note that the device was chosen due to the large effect the exposed paddle has on its thermal performance. The results shown can be much less drastic depending on the IC and its specifications.

The die is packaged in a 100-pin TQFP-EP (-EP denotes exposed paddle). A diode on the die was calibrated and then used to monitor the junction temperature.

A comparison of ambient temperature vs. device temperature for the different boards is given in Figure 9. Having the exposed paddle attached resulted in a 42.4% decrease in device temperature at 25°C ambient (Figure 9). The lower temperature also decreased power consumption of the IC by 4.6% (Figure 10).

The maximum junction temperature of this device is 150°C. As seen in Figure 9, the proper attachment of the exposed paddle is critical for proper operation of this device. Damage to the device could occur at ambient temperatures as low as 60°C if the exposed paddle is not connected correctly.

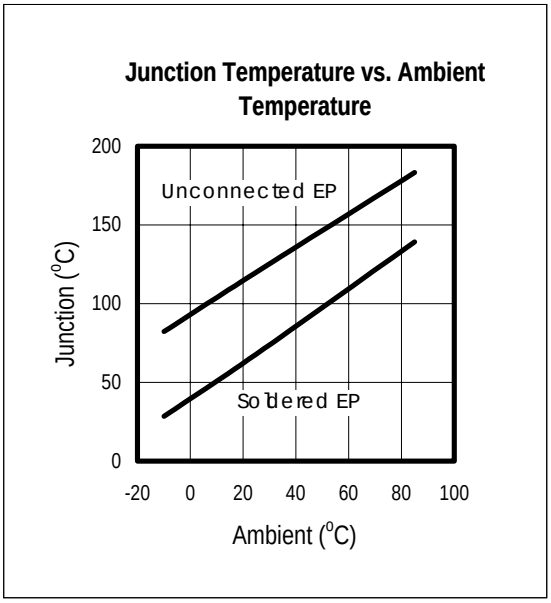

Figure 9: Ambient Temperature vs. Junction Temperature

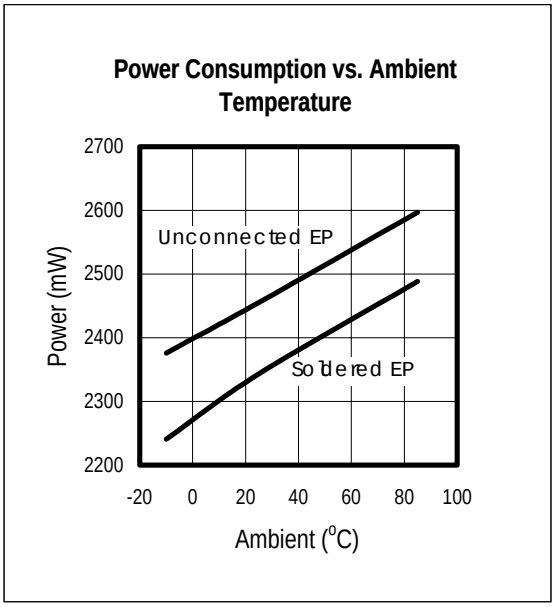

Figure 10. Power Consumption vs. Ambient Temperature

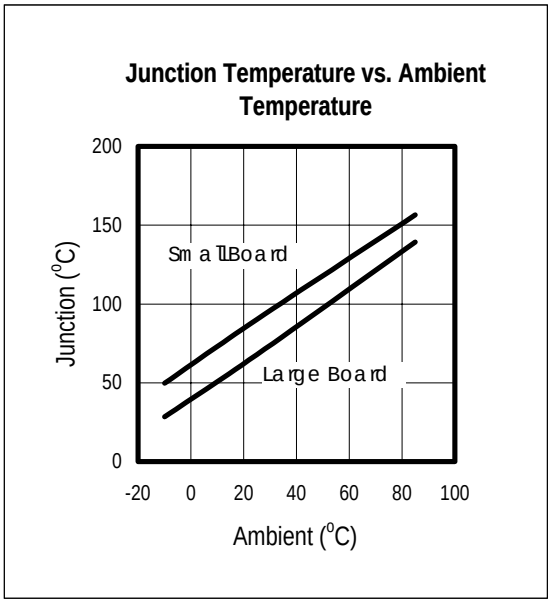

Figure 11: Ambient Temperature vs. Device Temperature

The relative size of ground plane and surrounding material is also an important consideration as its effects are shown in Figure 11. The large board has an approximate size of 370cm^2 compared to the small board of 14cm^2. The larger board resulted in 20°C drop in device junction temperature.

The θ_{JA} results from these tests are given in Table 2. Note that the θ_{JA} values given here are not the same as the θ_{JA} values for the package. θ_{JA} is very dependent on the characteristics of the system under test. The board and environment used for these tests were not JEDEC standard. The thermal resistance values are presented to show the relative change with changing system configurations.

Table 2: Thermal Resistance Example

Board Configuration	θ_{JA}
Unconnected EP	**39.91**
Soldered EP	
Large Board	**19.09**
Small Board	**28.14**

As seen from these experiments, proper use of the exposed paddle greatly improved the performance of the device. Incorrect use of the exposed paddle can lead to increased failure rate, decreased electrical performance or permanent thermal damage. Board size and proper soldering of the exposed paddle were shown to have a large effect on the overall thermal performance.

6 Summary

The exposed paddle greatly improves system level performance by increasing thermal dissipation, decreasing workable package size, and improving electrical performance. Proper soldering of the exposed paddle to a suitable thermally conductive surface, such as a ground plane, is critical in obtaining the improved performance of the exposed-paddle package and proper operation of the IC.

References:

1. A. Bar-Cohen, "Thermal Packaging for the 21st Century: Challenges and Options." International Workshop – Thermal Investigations of ICs and Systems; Rome, Italy; September 1999.

2. B. Guenin, "Packaging: Designing for Thermal Performance." *Electronics Cooling*, May 1997.

3. M. Okcay, "Thermal Interface Under a Plastic Quad Flat Pack." *Electronics Cooling*, May 1998.

4. R. Sengupta, T. Bandyopadhyay, "Thermal Management In Printed Wiring Assembly with Surface Mount Devices." *Instruments and Electronics*, July 1997.

5. Application Note: "Application Notes for Surface Mount Assembly of Amkor's Thermally Enhanced Lead Frame Based Packages." Amkor Technology, February 1999.

6. Application Note: "Application Notes for Surface Mount Assembly of Amkor's Micro Lead Frame (MLF) Packages." Amkor Technology, March 2001.

7. Technical Brief: "PowerPAD Thermally Enhanced Package." SLMA002, Texas Instruments Semiconductor Group, November 1997.

8. Application Note: "Thermal Derating Curves for Logic-Products Packages." SZA013A, Texas Instruments, March 1999.

9. Application Note: "Transient Thermal Resistance – General Data and Its Use." AN-569, Motorola Semiconductor Products Inc, 1973.

10. Application Note: "Appendix E: Understanding Integrated Circuit Package Power Capabilities." National Semiconductor, April 2000.

11. Application Note: "Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs." SZZA017A, Texas Instruments, September 1999.

Note: The following Standards can be downloaded from the JEDEC website,

http://www.jedec.org/DOWNLOAD/search/default2.cfm

12. JESD51: Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device).

13. JESD51-1: Integrated Circuit Thermal Measurement Method – Electrical Test Method (Single Semiconductor Device).

14. JESD51-2: Integrated Circuit Thermal Test Method Environmental Conditions – Natural Convection (Still Air).

15. JESD51-3: Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.

16. JESD51-4: Thermal Test Chip Guideline (Wire Bond Type Chip).

17. JESD51-5: Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms.

18. JESD51-6: Integrated Circuit Thermal Test Method Environmental Conditions – Forced Convection (Moving Air).

19. JESD51-7: High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.

20. JESD51-8: Integrated Circuit Thermal Conductivity Test Method Environmental Conditions – Junction-to-Board.

21. JESD51-9: Test Boards for Area Array Surface Mount Packages Thermal Measurements.

22. JESD51-10: Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements.